Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A low noise voltage regulator circuit for generating a stable voltage signal with low noise, the low noise voltage regulator circuit comprising:

a reference voltage generator, electrically coupled to a first node, for generating a first voltage signal and outputting the first voltage signal to the first node;

a switching circuit, electrically coupled to the first node, a second node, and a switching control signal, for receiving the first voltage signal from the first node, processing the first voltage signal to generate a second voltage signal, and outputting the second voltage signal to the second node, wherein the switching circuit switches between a first state and a second state, when the switching circuit is at the first state, it is substantially equivalent to a voltage follower, the first voltage signal is coupled to become the second voltage signal without being filtered, when the switching circuit is at the second state, it is substantially equivalent to a RC low pass filter, the first voltage signal is filtered to become the second voltage signal; and

a stabilizing circuit electrically coupled between the sec-

ond node and a third node and including a negative feedback path, the stabilizing circuit receives the second voltage signal from the second node and provides the stable voltage signal to the third node.

[c2] 2.The low noise voltage regulator circuit of claim 1, wherein the switching circuit comprises:
a resistor, electrically coupled between the first node and the second node;
a capacitor, electrically coupled between a fourth node and ground; and
a switch circuit, electrically coupled to the first node, the second node, the fourth node, and the switching control signal, the switch circuit can switch the switching circuit between the first state and the second state according to the switching control signal, when the switching circuit is at the first state, the switch circuit conducts the first node with the fourth node, when the switching circuit is at the second state, the switch circuit conducts the sec-ond node with the fourth node.

[c3] 3.The low noise voltage regulator circuit of claim 2, wherein the switch circuit comprises:
a first switch, electrically coupled between the first node and the fourth node, the switching control signal can turn on or turn off the first switch, when the switching circuit is at the first state, the switching control signal

turns on the first switch for conducting the first node with the fourth node, when the switching circuit is at the second state, the switching control signal turns off the first switch; and

a second switch, electrically coupled between the second node and the fourth node, the switching control signal can turn on or turn off the second switch, when the switching circuit is at the first state, the switching control signal turns off the second switch, when the switching circuit is at the second state, the switching control signal turns on the second switch for conducting the first node with the fourth node.

[c4] 4.The low noise voltage regulator circuit of claim 3, wherein:

the first switch is a PMOS transistor having the gate terminal electrically coupled to the switching control signal, the source terminal electrically coupled to the first node, and the drain terminal electrically coupled to the fourth node; and

the second switch is an NMOS transistor having the gate terminal electrically coupled to the switching control signal, the drain terminal electrically coupled to the second node, and the source terminal electrically coupled to the fourth node;

wherein when the switching circuit is at the first state,

the switching control signal is at a low potential, when the switching circuit is at the second state, the switching control signal is at a high potential.

[c5] 5.The low noise voltage regulator circuit of claim 4 further comprising an inverter chain with an even number of inverters serially coupled together, the input end being electrically coupled to the third node, the output end outputting the switching control signal according to the voltage of the third node and being electrically coupled to the gate of the PMOS transistor and the gate of the NMOS transistor.

[c6] 6.The low noise voltage regulator circuit of claim 3, wherein:
the first switch is an NMOS transistor having the gate terminal electrically coupled to the switching control signal, the drain terminal electrically coupled to the first node, and the source terminal electrically coupled to the fourth node;
the second switch is a PMOS transistor having the gate terminal electrically coupled to the switching control signal, the source terminal electrically coupled to the second node, and the drain terminal electrically coupled to the fourth node;
wherein when the switching circuit is at the first state, the switching control signal is at a high potential, when

the switching circuit is at the second state, the switching control signal is at a low potential.

[c7] 7.The low noise voltage regulator circuit of claim 6 further comprising an inverter chain with an odd number of inverters serially coupled together, the input end being electrically coupled to the third node, the output end outputting the switching control signal according to the voltage of the third node and being electrically coupled to the gate of the PMOS transistor and the gate of the NMOS transistor.

[c8] 8.The low noise voltage regulator circuit of claim 1, wherein the switching circuit comprises:
a resistor, electrically coupled between the first node and the second node;
a capacitor, electrically coupled between the second node and ground; and
a switch, electrically coupled between the first node and the second node, the switch switches the switching circuit between the first state and the second state according to the switching control signal, when the switching circuit is at the first state, the switching control signal turns on the switch to conduct the first node with the second node, when the switching circuit is at the second state, the switching control signal turns off the switch.

[c9] 9.The low noise voltage regulator circuit of claim 8, wherein the switch is an NMOS transistor having the gate terminal electrically coupled to the switching control signal, a first terminal electrically coupled to the first node, and a second terminal electrically coupled to the second node, when the switching circuit is at the first state, the switching control signal is at a high potential, when the switching circuit is at the second state, the switching control signal is at a low potential.

[c10] 10.The low noise voltage regulator circuit of claim 9 further comprising an inverter chain with an odd number of inverters serially coupled together, the input end of the inverter chain being electrically coupled to the third node, the output end outputting the switching control signal according to the voltage of the third node and being electrically coupled to the gate of the NMOS transistor.

[c11] 11.The low noise voltage regulator circuit of claim 8, wherein the switch is a PMOS transistor having the gate terminal electrically coupled to the switching control signal, a first terminal electrically coupled to the first node, and a second terminal electrically coupled to the second node, when the switching circuit is at the first state, the switching control signal is at a low potential, when the switching circuit is at the second state, the switching

control signal is at a high potential.

[c12] 12.The low noise voltage regulator circuit of claim 11 further comprising an inverter chain with an even number of inverters serially coupled together, the input end of the inverter chain being electrically coupled to the third node, the output end outputting the switching control signal according to the voltage of the third node and being electrically coupled to the gate of the PMOS transistor.

[c13] 13.A low noise voltage regulator circuit for generating a stable voltage signal with low noise, the low noise voltage regulator circuit comprising:
a reference voltage generator having a first node for providing a first voltage signal;
a stabilizing circuit having an input node and an output node, the stabilizing circuit includes a negative feedback path for providing the stable voltage signal at the output node;
an intermediate module coupled between the first node and the input node, the intermediate module having a first state and the second state, wherein when the intermediate module is at the first state the first voltage signal is coupled to the input node without being filtered, and when the intermediate module is at the second state the first voltage signal is coupled to the input node after

being filtered.